Canceled B6

parallel which are selectable individually and in parallel combinations to select different phase shift values.

Add the following new claims.

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34. The array of Claim 27, wherein the respective plurality of susceptances comprising said first and second reactance circuits define pairs of equal susceptances which are switched in tandem to provide symmetrical operation.

35. The circuit of Claim 31, wherein the respective plurality of selectable reactance values connected in parallel for the first and second termination reactance circuits define pairs of equal reactance values which are switched in tandem to provide symmetrical operation.

36. The circuit of Claim 33, wherein the respective plurality of selectable reactance values connected in parallel for the first and second termination reactance circuits define pairs of equal reactance values which are switched in tandem to provide symmetrical operation.

REMARKS

The Examiner is thanked for the careful review of the application as set out in the outstanding office action. Reconsideration of the application is respectfully requested.

A marked up version of the changes made to the application showing the changes made is attached hereto.

In the outstanding office action, Claims 5, 25 and 26 have been rejected under 35 USC § 102 as being anticipated by Loo et al. (Loo), Claims 9, 13, 14, 30 and 32 have been rejected under 35 USC § 103 as being unpatentable

over Loo in view of Hong, and Claims 21, 27, 28, 29, 31 and 33 have been rejected as being unpatentable over Nakahara in view of Loo and Hong.

Claims 9, 25, 30 and 32 have been cancelled without prejudice, and Claims 5, 14, 21, 27, 31 and 33 have been amended.

Claim 27 is drawn to an array including an array of reflection phase shifters, including a plurality of micro-electro-mechanical ("MEM") switches responsive to said control signals to select one of a discrete number of phase shift settings for the respective phase shifter, a coupler device having first and second RF I/O ports, and in-phase and quadrature ports, and first and second reactance circuits respectively coupled to the in-phase and quadrature ports by first and second MEM switch circuits, said first and second reactance circuits each comprising a plurality of susceptances connected in parallel for terminating said in-phase or quadrature port, and wherein first and second MEM switch circuits select at least one of said plurality of susceptances connected in parallel for each of said first and second reactance circuits to select a phase shift setting, and wherein said plurality of susceptances can be selected individually and in parallel combinations.

Nakahara, Loo and Hong, taken alone or in combination, do not disclose or suggest a reflection phase shifter having first and second reactance circuits as recited in Claim 27. Selecting individually and in parallel combinations of terminating susceptances is not taught or suggested by the applied art. The capability of selecting individual and parallel combinations of terminating susceptances increases the number of phase states for the phase shifter. Nakahara does not disclose the selection of parallel combinations of terminating susceptances, but only selection of one reactance leg or the other, or neither reactance leg. Loo and Hong do not disclose this feature either.

In order to achieve the same number of possible phase states provided by the phase shifter of Claim 27, Nakahara would need to add additional phase shifter stages connected in series, with a consequent increase in cost, size and loss.

Claims 28-29 depend from Claim 27, and further distinguish from the applied art. For example, Claim 28 recites that the MEM switch circuits comprise first, second and third MEM switches each terminated respectively in a first, second or third one of the susceptances. Claim 29 recites that the plurality of susceptances can be switched individually and in parallel combinations to provide at least eight different discrete phase settings. As noted by the Examiner, at page 8, last paragraph of the office action, Nakahara teaches adding additional stages in series to achieve increases in the number of phase states, and particularly would require a plurality of stages to obtain 8 phase states. The disadvantages of this approach include the increased cost, size and loss associated with increased numbers of phase shifter stages.

Claim 31 is drawn to an RF reflection phase shifter circuit, wherein the MEM switch circuit includes first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each said reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable individually and in parallel combinations to select different phase shift values. Nakahara, Loo and Hong, alone or in combination do not teach or suggest such a circuit.

Claim 33 is drawn to a multi-section RF phase shifter circuit, comprising:

a plurality of reflection phase shift sections connected in series to provide a discrete set of selectable phase shifts to RF signals passed through the circuit, and wherein each reflection phase shift section includes:

a coupler device having first and second RF I/O ports, and in-phase and quadrature ports;

a switch circuit comprising a plurality of single-pole-single-throw (SPST) micro-electro-mechanical ("MEM") switches responsive to control signals, said switch circuit arranged to select one of a plurality of discrete phase shift values introduced by the

phase shifter circuit to RF signals passed between the first and second RF ports;

said MEM switch circuit including first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each said reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable individually and in parallel combinations to select different phase shift values.

As discussed above, the applied references do not teach or suggest a MEM switch circuit including first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable individually and in parallel combinations to select different phase shift values. The rejection of Claim 33 should therefore be withdrawn.

New Claims 34-36

New Claim 34 depends from Claim 27, and further recites that the respective plurality of susceptances comprising the first and second reactance circuits define pairs of equal susceptances which are switched in tandem to provide symmetrical operation. This feature is fully supported by applicants' specification, e.g. at 19:11-14 and 21:23-32. These claims are also in condition for allowance.

CONCLUSION

The outstanding objections and rejections have been addressed, and the application is now in condition for allowance. Such favorable reconsideration is solicited.

Respectfully submitted,

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Leonard A. Alkov
Registration No. 30,021

Raytheon Company
Building - E1 M.S. 150
P.O. Box 902
El Segundo, CA 90245-0902
Telephone (310) 647-2577
Facsimile (310) 647-2616

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

5. (Twice Amended) The array of Claim [25] 27 wherein said MEM switches are single-pole-single-throw (SPST) switches including an armature for opening and closing the RF signal path through the switch, and a control signal path, and wherein the control signals are isolated from the RF signal path.

14. (Amended) The circuit of Claim [30] 31, wherein said MEM switches are metal-metal contact RF MEMS series switches.

21. (Twice Amended) The circuit of Claim 27, wherein said first and second MEM switch circuits provide MPMT (multiple-pole-multiple-throw) switching functions.

27. (Amended) An electronically scanned array, comprising:

a linear array of radiating elements;

an array of reflection phase shifters coupled to the radiating elements;

an RF manifold including a plurality of phase shifter ports respectively coupled to a corresponding phase shifter RF port and an RF port; and

a beam steering controller for providing phase shift control signals to the phase shifters to control the phase shift setting of the array of the phase shifters;

and wherein said phase shifters each include:

a plurality of micro-electro-mechanical ("MEM") switches responsive to said control signals to select one of a discrete number of phase shift settings for the respective phase shifter;

a coupler device having first and second RF I/O ports, and in-phase and quadrature ports, and first and second reactance circuits

respectively coupled to the in-phase and quadrature ports by first and second MEM switch circuits, said first and second reactance circuits each comprising a plurality of susceptances connected in parallel for terminating said in-phase or quadrature port, and wherein first and second MEM switch circuits select at least one of said plurality of susceptances connected in parallel for each of said first and second reactance circuits to select a phase shift setting, and wherein each of said plurality of susceptances can be selected individually and in parallel combinations.

31. (Amended) An RF reflection phase shifter circuit, comprising:

a coupler device having first and second RF I/O ports, and in-phase and quadrature ports;

a switch circuit comprising a plurality of single-pole-single-throw (SPST) micro-electro-mechanical ("MEM") switches responsive to control signals, said switch circuit arranged to select one of a plurality of discrete phase shift values introduced by the phase shifter circuit to RF signals passed between the first and second RF ports, said circuits connected to provide a single-pole-multiple-throw (SPMT) or multiple-pole-multiple-throw (MPMT) switch function;

said MEM switch circuit including first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each said reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable individually [or] and in parallel combinations to select different phase shift values.

33. (Amended) A multi-section RF phase shifter circuit, comprising:

a plurality of reflection phase shift sections connected in series to provide a discrete set of selectable phase shifts to RF signals passed through the circuit, and wherein each reflection phase shift section includes:

a coupler device having first and second RF I/O ports, and in-phase and quadrature ports;

a switch circuit comprising a plurality of single-pole-single-throw (SPST) micro-electro-mechanical ("MEM") switches responsive to control signals, said switch circuit arranged to select one of a plurality of discrete phase shift values introduced by the phase shifter circuit to RF signals passed between the first and second RF ports[, said circuits connected to provide a single-pole-multiple-throw (SPMT) or multiple-pole-multiple-throw (MPMT) switch function];

said MEM switch circuit including first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each said reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable individually [or] and in parallel combinations to select different phase shift values.